WHAT IS CLAIMED IS:

1. A method of fabricating a transistor having a source, drain, and a gate on a substrate, the method comprising:

implanting, into a surface of the substrate, a first impurity region (500A) with a first volume and a first surface area, the first impurity region being of a first type;

forming a gate oxide (508) between a source region and a drain region of the transistor;

covering the gate oxide with a conductive material (708A);

implanting, into the source region of the transistor, a second impurity region (518) with a second volume and a second surface area in the first surface area of the first impurity region, the second impurity region being of an opposite second type relative to the first type, wherein implanting the second impurity region includes,

a first implant (802) to limit a vertical depth of the second impurity region; and

a second implant (804) separate from the first implant to control a lateral channel length of the transistor;

implanting, into the source region of the transistor, a third impurity region (514) with a third volume and a third surface area and a fourth impurity region (516) with a fourth volume and a fourth surface area, in the second surface area of the second impurity region, the third impurity region being of the first type, the fourth impurity region being of the opposite second type; and

implanting, into the drain region of the transistor, a fifth impurity region (510) with a fifth volume and a fifth surface area, the fifth impurity region being of the first type.

2. The method of claim 1, wherein:

the first implant to limit the vertical depth of the second impurity region occurs prior to formation of the gate oxide of the transistor; and

the second implant to control the lateral channel length of the transistor occurs after the formation of the gate oxide of the transistor.

3. The method of claim 1, wherein the first implant to limit the vertical depth of the second impurity region and the second implant to control the lateral channel length of the transistor both occur after formation of the gate oxide of the transistor.

4. The method of claim 1, wherein the first implant is a high energy implant.

5. The method of claim 1, wherein the first implant is a large angle tilt implant.

6. The method of claim 1, wherein the first implant is deeper than the second implant.

7. The method of claim 1, further comprising implanting, into the drain region of the transistor, a sixth impurity region (512) with a sixth volume and a sixth surface area in the first surface area of the first impurity region, the sixth impurity region being implanted with a spacing from the second impurity region, the sixth impurity region being of the first type.

8. The method of claim 10, wherein the sixth impurity region is self aligned to the gate of the transistor and is implanted after forming the gate oxide of the transistor.

9. The method of claim 10, wherein the sixth impurity region is non-self aligned to the gate of the transistor and is implanted prior to forming of the gate oxide of the transistor.

10. The method of claim 10, wherein the spacing of the second impurity region from the sixth impurity region is sized such that the sixth impurity region is spaced a distance (*d*) away from the gate of the transistor as measured along a surface of the transistor.

11. The method of claim 10, wherein the first impurity region and the sixth impurity region are implanted using a same mask.

12. The method of claim 10, wherein the implantation of the fifth impurity region is defined by a slit mask, the fifth impurity region forming multiple implants (1812) spaced apart relative to each other along a surface of the transistor in the drain region of the transistor.

13. The method of claim 12, wherein the third impurity region, the fifth impurity region and the sixth impurity region are implanted simultaneously using the slit mask.

14. The method of claim 1, further comprising implanting, into the source region of the transistor a seventh impurity region (1704) with a seventh volume having a seventh surface area, and implanting, into the drain region of the transistor, an eighth impurity region (1706) with an eighth volume having an eighth surface area, the seventh impurity region and the eighth impurity region being of the first type.

15. The method of claim 1, further comprising:
forming a field oxide (2702) on the drain region of the transistor.

16. The method of claim 1, wherein the transistor is an LDMOS transistor.